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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/944,830	08/31/2001	Mark Alan Lemkin	AIMI-01841US0	3407

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EXAMINER
HUYNH, ANDY

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 01/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/944,830	LEMKIN, MARK ALAN	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-76* is/are pending in the application.

4a) Of the above claim(s) *32-59* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19,21-25,27-31 and 60-76* is/are rejected.

7)☒ Claim(s) *20 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. In Election/Restrictions Response, Applicants have elected Group I (claims 1-31 and 60-74), and amended claims 75 and 76 in Paper No. 8 dated December 30, 2002, and in view of the amendments to claims 75 and 76, claims 75 and 76 are now regrouped with claims 1-31 and 60-76 is acknowledged. Claim 59 is withdrawn from consideration as being directed to a non-elected invention. Accordingly, claims 1-31 and 60-76 are pending in this application.

Information Disclosure Statement

2. This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed on August 31, 2001 and made of record as Paper No. 2. The references cited on the PTOL 1449 form have been considered.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims **21-24, 28, and 71-73** are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim **21**, the claim recites the limitation "the maximum thickness" is indefinite, since it is not disclosed in the specification and unclear.

Claims **22-24** depend from the rejected claim 21 and include all of the limitations of claim 21 thereby rendering these dependent claims indefinite.

Regarding claim **28**, the claim recites the limitation "an input voltage". There is insufficient antecedent basis for this limitation in the claim **25**.

Regarding claims **71 and 73**, the claim recites the limitations "said current-steering circuit" and "said reference circuit". There is insufficient antecedent basis for these limitations in the claim **68**.

Regarding claim **72**, the claim recites the limitation "said reference circuit". There is insufficient antecedent basis for this limitation in the claim **69**.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim **1** is rejected under 35 U.S.C. 102(b) as being anticipated by Todokoro (USP: 4,021,747).

Todokoro discloses in Fig. 4 a circuit/signal amplifier circuit for quantifying a high-voltage signal comprising:

a first terminal 14 having a first voltage IN;

an output terminal 13;

a field transistor Q1 having a drain, a gate, and a source, said gate connected to said first terminal, said drain and source having a second and third voltage, said output terminal coupled to said field transistor;

wherein said output terminal provides a signal representative of said first voltage (col. 5, lines 29-52).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5. Claims **14-16, 25 and 29** are rejected under 35 U.S.C. 102(e) as being anticipated by Lopata (USP: 6,265,941).

Regarding claim **14**, Lopata discloses in Fig. 2 a circuit comprising:

at least one low voltage input 14;

a first high voltage terminal 12; and

a first filed transistor 2T1 having a source, a drain, and a control region;

wherein the control region is coupled to the first high voltage terminal (col. 2, lines 38-48).

Regarding claim **15**, Lopata discloses in Fig. 2 the circuit further includes a second field transistor 2T2 coupled to the first field transistor.

Regarding claim **16**, Lopata discloses in Fig. 2 each field transistor includes a cascode transistor 2T5, 2T6 coupled thereto.

Regarding claims **25** and **29**, Lopata discloses in Fig. 2 the circuit further including a second field transistor 2T2, each field transistor having coupled thereto a cascode transistor 2T5, 2T6 and a mirror transistor 2T3, 2T4, wherein each field transistor is coupled to a first rail VDD and each mirror transistor is coupled to a second rail GND and the gate of each cascode transistor is coupled to a cascode voltage.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims **2-4** are rejected under 35 U.S.C. 103(a) as being unpatentable over Todokoro (USP: 4,021,747) in view of Lin (USP: 5,502,009).

Regarding claim **2**, Todokoro discloses the claimed invention except for the filed transistor further comprises a polysilicon gate; and a gate oxide; wherein said gate oxide is formed during a LOCOS step including a masked region masked by silicon-nitride, said gate oxide formed in a region absent of silicon-nitride.

Lin teaches in Figs. 1D and 2A-2D that the filed transistor comprises a polysilicon gate 16 (Fig. 1D, col. 2, lines 1-6); and a gate oxide 14, 15, 23, 26; wherein said gate oxide is formed

during a LOCOS step including a masked region masked by silicon-nitride 24, said gate oxide formed in a region absent of silicon-nitride (col. 3, lines 5-60).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the field transistor includes a polysilicon gate; and a gate oxide; wherein said gate oxide is formed during a LOCOS step including a masked region masked by silicon-nitride, said gate oxide formed in a region absent of silicon-nitride, as taught by Lin, since it was known in the art that the field transistor could be used to incorporate into Todokoro's structure to form the claimed invention.

Regarding claims **3 and 4**, Todokoro and Lin disclose the claimed invention except for the gate oxide has a thickness of at least 0.1 micron or 0.5 micron. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the filed transistor with the gate oxide having a thickness of at least 0.1 micron or 0.5 micron, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

7. Claim **5** is rejected under 35 U.S.C. 103(a) as being unpatentable over Todokoro (USP: 4,021,747) in view of Xiang et al. (USP: 6,187,657, hereinafter "Xiang").

Todokoro discloses the claimed invention except for the field transistor comprises a metal gate layer deposited over a thermal oxide. The field transistor including a metal gate layer deposited over a thermal oxide is known in the art. Xiang teaches that a field-effect transistor (FET) containing a metal gate over thermal oxide over silicon (MOSFET) (see col. 1, lines 5-12). It would have been obvious to one of ordinary skill in the art at the time of the invention was

made to utilize the field transistor comprising a metal gate layer deposited over a thermal oxide to incorporate into Todokoro's structure to form the claimed invention.

8. Claims **6 and 13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Todokoro (USP: 4,021,747) in view of Xiang et al. (USP: 6,187,657, hereinafter "Xiang") further in view of Rasovsky et al. (USP: 6,362,508, hereinafter "Rasovsky").

Regarding claim **6**, Todokoro and Xiang disclose the claimed invention except for a thick, oxide layer deposited as a pre-metal dielectric after poly deposition above the active region.

Rasovsky teaches in Fig. 1 that a pre-metal dielectric 150 is deposited after poly deposition 120 above the active region 110A, 110B (col. 3). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize a pre-metal dielectric after poly deposition above the active region as taught by Rasovsky in order to provides both memory retention and facilitates CMP planarization to incorporate into Todokoro and Xiang's structure to form the claimed invention.

Regarding claim **13**, Todokoro and Xiang disclose the claimed invention except for the field transistor further includes a drain extension region formed under the active region by a dopant species implanted into said active region.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the field transistor further including a drain extension region formed under the active region by a dopant species implanted into said active region since it was known in the art that the dopant species may be N-type impurity (e.g. phosphorus) for NMOS devices or P-

type impurity (e.g. boron) for PMOS devices used to implant into the active region to form source/drain regions or source/drain extension regions.

9. Claim **7** is rejected under 35 U.S.C. 103(a) as being unpatentable over Todokoro (USP: 4,021,747) in view of Xiang et al. (USP: 6,187,657, hereinafter "Xiang") further in view of Goo (USP: 6,362,508).

Todokoro and Xiang disclose the claimed invention except for a deposited oxide which lies upon a LOCOS oxide.

Goo teaches in Fig. 3D a deposited oxide 47 which lies upon a LOCOS oxide 42 (col. 5, lines 25-29). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize a deposited oxide which lies upon a LOCOS oxide as taught by Goo to acts as a blocking means which limits the implantation of the impurity ions (col. 5, lines 59-61) to incorporate into Todokoro and Xiang's structure to form the claimed invention.

10. Claims **8-11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Todokoro (USP: 4,021,747) in view of Rasovsky et al. (USP: 6,362,508, hereinafter "Rasovsky").

Rasovsky discloses in Fig. 1 the field transistor comprises a NMOS transistor 110B formed over a p-type region/P-WELL 105, a PMOS transistor 110A formed over an n-type region/N-WELL 103.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the field transistor comprising a NMOS transistor formed over a p-type/P-WELL region, or comprising a PMOS transistor formed over an n-type/N-WELL region as taught by Rasovsky in order to form MOS devices or CMOS devices to utilize in the claimed invention since the MOS/CMOS devices are well-known in the semiconductor art.

11. Claim **12** is rejected under 35 U.S.C. 103(a) as being unpatentable over Todokoro (USP: 4,021,747) in view of Lin (USP: 5,502,009) further in view of Schrantz (USP: 5,008,719).

Todokoro and Lin disclose the claimed invention except for the field transistor further includes a drain extension region formed under said gate oxide by a dopant species introduced before said LOCOS step.

Schrants teaches that a LOCOS process requires that source and drain extensions be implanted prior to the formation of the LOCOS regions (col. 5, lines 51-53).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the field transistor further including a drain extension region formed under said gate oxide by a dopant species introduced before the LOCOS step as taught by Schrants to incorporate into Todkoro and Lin's teachings to form the claimed invention in order to prevent channel length to be prone to misalignment-induced variation due to the LOCOS regions are not self-aligned to the extensions (col. 5, lines 53-56).

12. Claims **17-19, 27, 30-31 and 66-69** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lopata (USP: 6,265,941).

Regarding claims **17 and 18**, Lopata discloses the claimed invention except for the first field transistor comprises a NMOS or PMOS transistor. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the first field transistor comprising a NMOS or PMOS transistor in the claimed invention since the NMOS and PMOS transistors are well-known in the semiconductor art.

Regarding claim **19**, Lopata discloses the claimed invention except for each field transistor has a width, and wherein said second field transistor has a width which is greater than

the width of the first field transistor. It would have been an obvious matter of design choice to utilize each field transistor having a different width for a different voltage threshold, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955).

Regarding claim **27**, Lopata discloses the claimed invention except for the circuit wherein the first high voltage terminal has a swing of at least 40v. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to set the first high voltage terminal having a swing of at least 40v since it was known in the art that high voltage amplifiers (i.e. amplifiers having a voltage swing of greater than about 40-60v) typically require a highly specialized circuit technology to withstand substantial voltage differences (see Description of the Related Art of the application).

Regarding claim **30**, Lopata discloses the claimed invention except for the circuit wherein the mirror transistor coupled to the first field transistor is a diode connected input to a current mirror. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the mirror transistor coupled to the first field transistor is a diode connected input to a current mirror, since it has been held that omission of an element and its function in a combination where the remaining elements perform the same function as before involves only routine skill in the art In re Karlson, 136 USPQ 184.

Regarding claim **31**, Lopata discloses in Fig. 2 the circuit wherein the second field transistor 2T2 is connected to a mirror output 2T3.

Regarding claim **66**, Lopata discloses the claimed invention except for the circuit wherein the first high voltage terminal includes an amplified representation of said low voltage input. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the first high voltage terminal includes an amplified representation of the low-voltage input since it was known in the art that the amplified representation such as an amplifier is used to enhance a low-voltage signal.

Regarding claims **67 and 68**, Lopata discloses in Fig. 2 the circuit further including a diiferential mode feedback circuit 28. Lopata does not disclose the circuit including a second high voltage terminal. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include a second high voltage terminal to produce a differential voltage between the first and second high voltage terminal for comparison. Also, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have the differential voltage including an amplified representation of the low-voltage input since it was known in the art that the amplified representation such as an amplifier is used to enhance a low-voltage signal.

Regarding claim **69**, Lopata discloses in Fig. 2 the circuit further including a common mode feedback circuit 30.

13. Claims **60-62** are rejected under 35 U.S.C. 103(a) as being unpatentable over Todokoro (USP: 4,021,747).

Regarding claims **60-61**, Todokoro does not disclose exactly the signal representative of the first voltage is a voltage signal or a current. It is inhering that the signal representative of the

first voltage could be represented by a voltage signal or a current would have same characteristic of the signal, so it is obvious.

Regarding claim **62**, Todokoro discloses in Fig. 10A-10B, the circuit further including a low-voltage input 14B. Todokoro fails to disclose the first terminal includes an amplified representation of the low-voltage input. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the first terminal includes an amplified representation of the low-voltage input since it was known in the art that the amplified representation such as an amplifier is used to enhance a low-voltage signal.

14. Claims **63, 65, 70 and 74** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lopata (USP: 6,265,941) in view of Bee (USP: 5,426,396).

Regarding claims **63 and 65**, Lopata discloses the claimed invention except for the circuit further including a current-differencing circuit coupled to said first field transistor and said second field transistor, said current-differencing circuit having an output, and the current-differencing circuit further including a first input current; a second input current; wherein said output of said current-differencing circuit includes an amplified signal representative of the difference between said first input current and said second input current. Bee teaches that it is known to use a current-difference circuit as set forth in Abstract. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use a current-difference circuit including a first input current; a second input current; wherein said output of said current-differencing circuit includes an amplified signal representative of the difference between said first input current and said second input current to incorporate into the circuit, as taught by Bee in order to compare the current flowing between circuit nodes with a reference current to

produce an output signal representative of the applied signal which is selected in response to an applied control signal (see, Bee, Abstract).

Regarding claim **70**, Lopata discloses the claimed invention except for the circuit of further including a reference circuit; a current-steering circuit having an input and an output. Bee teaches that it is known to use a current-difference circuit as set forth in Abstract. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include a reference circuit for signal voltage comparison and use a current-difference circuit including a first input current; a second input current; wherein said output of said current-differencing circuit includes an amplified signal representative of the difference between said first input current and said second input current to incorporate into the circuit, as taught by Bee in order to compare the current flowing between circuit nodes with a reference current to produce an output signal representative of the applied signal which is selected in response to an applied control signal (see, Bee, Abstract).

Regarding claim **74**, Lopata does not disclose the circuit further comprising at least one MEMS mirror coupled to the high-voltage terminal. It would have been an obvious matter of design choice to include at least one MEMS mirror coupled to the high-voltage terminal, since applicant has not disclosed that MEMS mirror solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well without the MEMS mirror.

15. Claim **64** is rejected under 35 U.S.C. 103(a) as being unpatentable over Lopata (USP: 6,265,941) in view of Bee (USP: 5,426,396) further in view of Pullela et al. (US Pub. No. 2002/0135410 A1, hereinafter "Pullela").

Lopata and Bee disclose the claimed invention except for the circuit further including a trans-impedance stage having an input and an output, said trans-impedance stage input coupled to said current-differencing circuit output. Pullela teaches that it is known a trans-impedance stage may be used as an active load (see Pullela, claim 2). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use a trans-impedance stage to incorporate into the circuit, as taught by Pullela in order to use as an active load.

16. Claims **75 and 76** are rejected under 35 U.S.C. 103(a) as being unpatentable over Todokoro (USP: 4,021,747) in view of Bee (USP: 5,426,396).

Regarding claims **75 and 76**, Todokoro discloses the claimed invention except for the circuit of further including a reference circuit; a current-steering circuit having an input and an output coupled to the reference circuit. Bee teaches that it is known to use a current-difference circuit as set forth in Abstract. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include a reference circuit comprising at least a second transistor for signal voltage comparison and use a current-difference circuit including a first input current; a second input current; wherein said output of said current-differencing circuit includes an amplified signal representative of the difference between said first input current and said second input current to incorporate into the circuit, as taught by Bee in order to compare the current flowing between circuit nodes with a reference current to produce an output signal representative of the applied signal which is selected in response to an applied control signal (see, Bee, Abstract).

Allowable Subject Matter

17. Claims **20 and 26** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Lopata fails to teach the claimed invention the circuit having the width of the second field transistor is about 10 times greater than that of the first field transistor as recited in claim **20**; the circuit having the width of the second field transistor is greater than that of the first field transistor, such that a bias applied to the cascode transistors generates a gain between said drain currents dependent upon the ratio of the width of the second transistor to the first transistor as recited in claim **26**.

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Giles et al.'751, Ivanov et al.'153, Murray et al.'326, Tran et al.'267, Embree'892, Tien et al.'333, and Tero'378 are cited as of interest.

19. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (703) 305-0089. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM. The examiner's supervisor, David Nelms can be reached on (703) 308-4910. The Fax number for the organization where this application

or proceeding is assigned is (703) 308-7724. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

AH

David Nelms
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